Design and implementation of an efficient OFDM communication using fused floating point FFT

Pamidi Lakshmi Amrutha Valli [1] , Sunkara Rambadu [2] , V G Prasad Naraharasetti [3]
(M.Tech Student in VLSI [1], Asst.Professor [2], Asso.Professor& Head of the Department [3], ECE Department, S.I.T.E, Tadepalligudem, India)

***ABSTRACT**:*

In this paper, OFDMA scheme is proposed for multi-user wireless communications with specific application in all domains. A new VLSI architecture for real-time FFT processor is proposed in this paper. This concept introduces OFDM system using a programmable fused-point DSP.A reduced complexity software implementation of the technique is proposed and discussed. Both the interoperability and adaptability among modulation operational modes of the OFDM systems is supported. Here, fused floating point FFT is studied and implemented in method employing radix-4 decimation-in-time fast Fourier transform (FFT) algorithms.

Keywords- Fused floating point FFT, Orthogonal frequency division multiplexing(OFDM), Quadrature amplitude modulation(QAM), Fast Fourier transform(FFT), Inverse fast Fourier transform(IFFT), serial to parallel converter(S/P), parallel to serial converter(P/S).

INTRODUCTION

Two major problems associated with data communications over terrestrial wireless channels are inter symbol interference and fading caused by multipath propagation. In multi user applications such as personal mobile communications, other-user interference could also limit the system performance and capacity. In this paper, an interference tolerant wideband multiple access scheme is discussed based on the orthogonal frequency division multiplexing (OFDM). The scheme is designed as such, the amount of other-user interference and inter symbol interference are reduced. This is achieved using both a cyclic prefix and a cyclic suffix in the transmit data frames and noting that the Fourier code words used in OFDM have a zero cross correlation on all cyclic shifts.

Baseband OFDM Transmitter:

The OFDM transmitter can be implemented by using a regular IFFT, but without dividing the outputs by *N* as follows:

$$x_k = \sum_{n=0}^{N-1} d_n \cdot e^{j\frac{2\pi}{N}nk} \quad k = 0,1,\ldots,N-1$$

Where d_n is the predefined data symbol from bit stream b_n and $e^{j2\pi nk/N}$, *n*=0, 1… *N*-1, represents the corresponding orthogonal frequencies of the *N* sub-carriers. Fig. 4 shows a simplified OFDM transmitter block diagram. Note that the S/P is the serial-to-parallel converter and P/S is the parallel-to-serial converter.

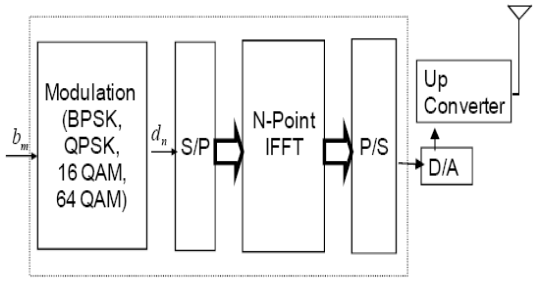


Figure 1: Block diagram of simplified OFDM transmitter

After P/S, the digital signal stream is then passed through the digital-to-analog (D/A) converter, frequency up converted with a carrier, and transmitted wirelessly[10].

QPSK Modulated Signal:

QPSK waveform is another form of angle-modulation where four output phases are possible for a single carrier frequency [10]. With the four different output phase possibilities, there must also be four corresponding input conditions (00, 01, 11, 10), which enjoy for the Gray code QPSK system to transmit twice as many data bits as the BPSK system with the same transmission bandwidth. Two serial bits b0b1 form a QPSK symbol. The b0 bit is used to encode the in-phase axis "I" and b1 bit is used to encode the quadrature axis "Q". QPSK signal constellation with Gray coding is illustrated in Fig. 2

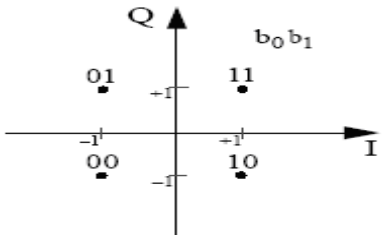


Figure 2: QPSK Signal Constellations with gray Coding

Quadrature Amplitude Modulation

Ability of equipment to distinguish small differences in phase limits the potential bit rate. This can be improved by combining ASK and PSK. This combined modulation technique is known Quadrature Amplitude Modulation (QAM). It is possible to obtain higher data rate using QAM. The constellation diagram of a QAM signal with two amplitude levels and four phases is shown in Fig. 3. It may be noted that M-ary QAM does not have constant energy per symbol, nor does it have constant distance between possible symbol values.

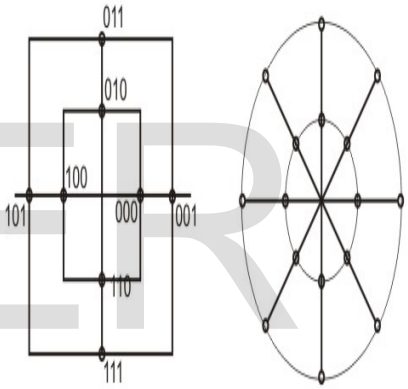


Figure 3: Constellation diagram for a QAM signal

Serial-Parallel Converter

The bits from the convolution coder is accepted serially by the serial to parallel converter and converted into parallel bits. Four bit control code is used. According to control code, each bit is assigned serially to temp data. All the bits in the temp data are grouped together to parallel data.

Parallel –Serial Converter

The parallel bits from IFFT can be converted into serial bits by using the parallel to serial converter. The input bits are stored in the shift registers. Each bit in the shift register is shifted right.

The bits that are shifted right are stored in register.

Baseband OFDM Receiver

The simplified receiver architecture is depicted in Fig. 4. At the receiver, the received signal is down converted and digitized via the analog-to-digital (A/D) converter. Assuming that the synchronization process has performed, the digital sampled signal r_k is passed through S/P, FFT processing, P/S, and demodulation operation. The final detected signal $\hat{d}_n$ of the *m*th OFDM symbol in additive white Gaussian noise (AWGN) channel is represented as follows.

$$\hat{d}_n = \frac{1}{N}\sum_{k=0}^{N-1} r_k e^{-j\frac{2\pi nk}{N}}, \quad n = 0,1,\ldots,N-1$$

Where,

$r_k = r_{k,m} = x_k + w_k$

Note that w_k is the AWGN and the OFDM symbol period is *T* where *T* = *NTs*. The detected bit $\hat{b}_m$ is obtained after the demodulation. Again all baseband operations inside the dashed box are software-based processing modules as depicted in Fig. 5

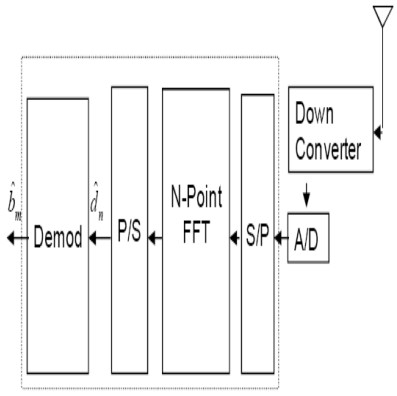


Figure 4 : Block diagram of simplified OFDM receiver

FFT and IFFT

As shown in Figs 1 and 4, the IFFT and FFT are the most time consuming part of the base-band OFDM processing for transmitter and receiver, respectively. Note that the IFFT operation can be performed using the FFT operation depicted in Fig. 5. By swapping the real and imaginary parts of the input sequence and swapping the real and imaginary parts of the output sequence, the FFT function is employed for the IFFT computation. Hence, if the OFDM transceiver is operated in time division multiplexing (TDM) mode, there is no additional hardware or software required for using the OFDM transmitter and receiver separately [9].

FUSED FLOATING-POINT DOT-PRODUCT UNIT AND ADD-SUBTRACT UNIT:

A floating-point fused dot-product unit **[1]** shown in fig 5. is presented that performs single-precision floating-point multiplication and addition operations on two pairs of data in a time that is only 150% the time required for a conventional floating-point multi -plication.

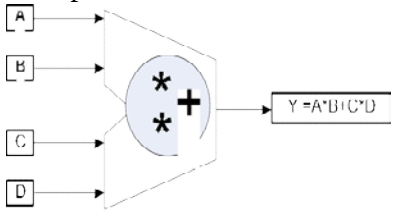


Figure 5: Fused DOT-PRODUCT Unit

The floating-point fused add-subtract unit (Fused AS) performs an addition and a subtraction in parallel on the same pair of data

$X = A + B$ and

$Y = A - B.$

The fused add-subtract unit is based on a conventional floating-point adder [1][3].

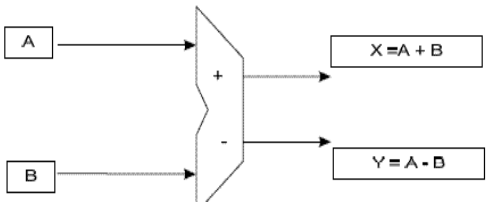


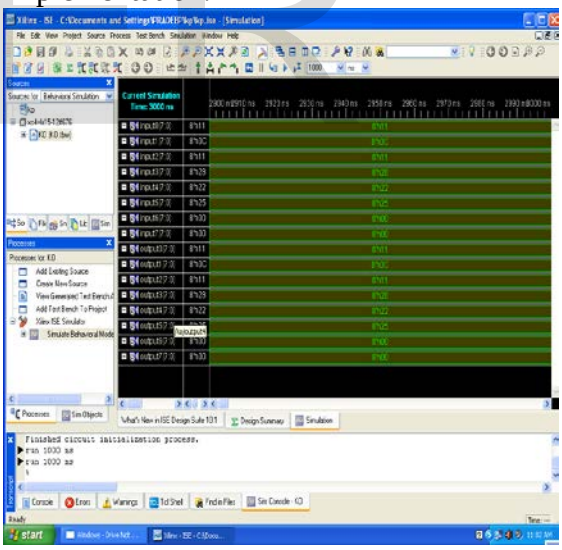
Figure 6: Fused ADD-SUB Unit

Although higher speed adder designs are available, the basic design shown here serves to demonstrate the concept. A block diagram of the fused add-subtract unit is shown in Fig.6.

Some details, such as the LZA and normalization logic are omitted here to simplify the figure. The exponent difference calculation, significant swapping, and the significant shifting for both the add and the subtract operations are performed with a single set of hardware and the results are shared by both the operations. This significantly reduces the required circuit area. The significant swapping and shifting is done based solely on the values of the exponents (i.e., without comparing the significants). As a result, if the exponents are equal, the smaller significand may be misidentified as the larger operand In other words, one DSP should be able to handle both IFFT and FFT operations if its throughput is fast enough. Due to the simplicity, the radix-16, decimation-in-time FFT algorithm is chosen, implemented, and used for both IFFT and FFT operation at the transmitter and receiver, respectively. The "butterfly" is the smallest computational unit and implemented by assembly code[13].

Results and Conclusion:

This paper describes the design of two new fused floating-point arithmetic units and their application to the implementation of FFT and IFFT butterfly operations along with whole OFDM system. Although the fused add-subtract unit is specific to FFT applications, the fused dot product is applicable to a wide variety of signal processing applications. Both the fused dot product unit and the fused add-subtract unit are smaller than parallel implementations constructed with discrete floating-point adders and multipliers. The fused dot product is faster than the conventional implementation, since rounding and normalization is not required as a part of each multiplication. Due to longer interconnections, the fused add-subtract unit is slightly slower than the discrete implementation.



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